at least one respective P-type source region formed in each of said body regions in said upper surface of said substrate and defining a respective channel region in said upper surface in said N-type body region;

a gate electrode disposed atop and insulated from said channel region and operable to invert said channel region in response to the application of a suitable gate voltage to said gate electrode; and

a source electrode disposed atop said [first] upper surface and connected to [each of] said at least one P-type source [regions] region;

said gate electrode being comprised of P-type polysilicon.

4. (Amended) The MOS gated device of claim 1 wherein each of said N-type channel regions has a doping concentration corresponding to that of an approximately 100 KeV phosphorus implant at a dose of about [5.5E13] $5.5x10^{13}$ atoms/cm^2.

5. (Amended) The MOS gated device of claim 1 wherein each of said N-type channel regions has a doping concentration corresponding to that of an approximately 100 KeV phosphorus implant at a dose of about [8.0E13] $8.0x10^{13}$ atoms/cm^2.

7. (Amended) The MOS gated device of claim 1 wherein at least one of said [base region] N-type body regions includes a portion adjacent to said upper surface that is more heavily doped than another portion of said [base region] N-type body regions that is adjacent to a lower boundary between said [base] N-type body region and said substrate.

13. (Amended) The MOS gated device of claim 1 wherein said gate electrode has a doping concentration corresponding to that of an approximately 50 KeV boron implant of about [5E15] $5x10^{15}$ atoms/cm^2.

APPENDIX C

complete set of "clean" claims

pursuant to 37 C.F.R. §1.121(c)(3)

1. A MOS gated device which is resistant to single event radiation failure and having improved total dose radiation resistance; said device comprising:

a P-type substrate having substantially flat, parallel upper and lower surfaces;

a plurality of laterally spaced N-type body regions extending from said upper surface into said substrate;

at least one respective P-type source region formed in each of said body regions in said upper surface of said substrate and defining a respective channel region in said upper surface in said N-type body region;

a gate electrode disposed atop and insulated from said channel region and operable to invert said channel region in response to the application of a suitable gate voltage to said gate electrode; and

a source electrode disposed atop said upper surface and connected to said at least one P-type source region;

said gate electrode being comprised of P-type polysilicon.

2. The MOS gated device of claim 1 in which said gate electrode is insulated from said channel region by a gate dielectric layer comprised of silicon dioxide.

3. The MOS gated device of claim 2 wherein said gate dielectric has a thickness of between 500 to 1000Å.

4. The MOS gated device of claim 1 wherein each of said N-type channel regions has a doping concentration corresponding to that of an approximately 100 KeV phosphorus implant at a dose of about 5.5×10^{13} atoms/cm^2.

5. The MOS gated device of claim 1 wherein each of said N-type channel regions has a doping concentration corresponding to that of an approximately 100 KeV phosphorus implant at a dose of about $8.0x10^{13}$ atoms/cm^2.

6. The MOS gated device of claim 1 wherein said substrate includes a chip of monocrystalline silicon at said lower surface of said substrate and an epitaxial layer formed atop said chip and that is less heavily doped than said chip.

7. The MOS gated device of claim 1 wherein at least one of said N-type body regions includes a portion adjacent to said upper surface that is more heavily doped than another portion of said N-type body regions that is adjacent to a lower boundary between said N-type body region and said substrate.

8. The MOS gated device of claim 1 further comprising an interlayer dielectric layer formed atop said gate electrode and having openings therein in which said source electrode contacts said source regions.

9. The MOS gated device of claim 8 wherein said interlayer dielectric is low temperature oxide.

10. The MOS gated device of claim 8 wherein said interlayer dielectric includes dopant ions.

11. The MOS gated device of claim 1 further comprising a passivation layer formed atop said source electrode.

12. The MOS gated device of claim 11 wherein said passivation layer is comprised of low temperature oxide.

13. The MOS gated device of claim 1 wherein said gate electrode has a doping concentration corresponding to that of an approximately 50 KeV boron implant of about $5x10^{15}$ atoms/cm^2.